L9951
L9951XP

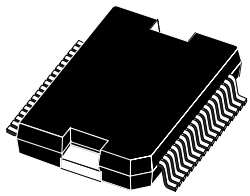
Rear door actuator driver

Features

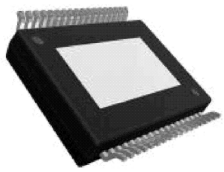
Type	Outputs[1]	R_{on}[2]	I_{OUT}	V_S
L9951 L9951XP	OUT1	150mΩ	7.4A	28V
	OUT2	200mΩ	5A	
	OUT3	200mΩ	5A	
	OUT4	800mΩ	1.25A	
	OUT5	800mΩ	1.25A	

1. See block diagram.
2. Typical values.

- One half bridge for 7.4 A load (R_{on} = 150 mΩ)
- Two half bridges for 5 A load (R_{on} = 200 mΩ)
- Two highside drivers for 1.25 A load (R_{on} = 800 mΩ)
- Programmable softstart function to drive loads with higher inrush currents (i.e.current > 7.4A, >5A, >1.25A)
- Very low current consumption in stand-by mode (I_S < 3µA, typ. T_j ≤85°C)
- All outputs short circuit protected
- Current monitor output for all highside drivers
- All outputs over temperature protected
- Open load diagnostic for all outputs
- Overload diagnostic for all outputs
- Programmable PWM control of all outputs
- Charge pump output for reverse polarity protection



PowerSO-36



PowerSSO-36

Application

Rear door actuator driver with bridges for door lock and safe lock and two 5W or 10W - light bulbs.

Description

The L9951 / L9951XP are microcontroller driven multifunctional rear door actuator driver for automotive applications. Up to two DC motors and two grounded resistive loads can be driven with three half bridges and two hide side drivers. The integrated standard serial peripheral interface (SPI) controls all operation modes (forward, reverse, brake and high impedance). All diagnostic informations are available via SPI.

Table 1. Device summary

Package	Order codes	
	Part number (Tube)	Part number (Tape & Reel)
PowerSO-36	L9951	L9951TR
PowerSSO-36	L9951XP	L9951XPTR

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1 Block diagram and pin description

Figure 1. Block diagram

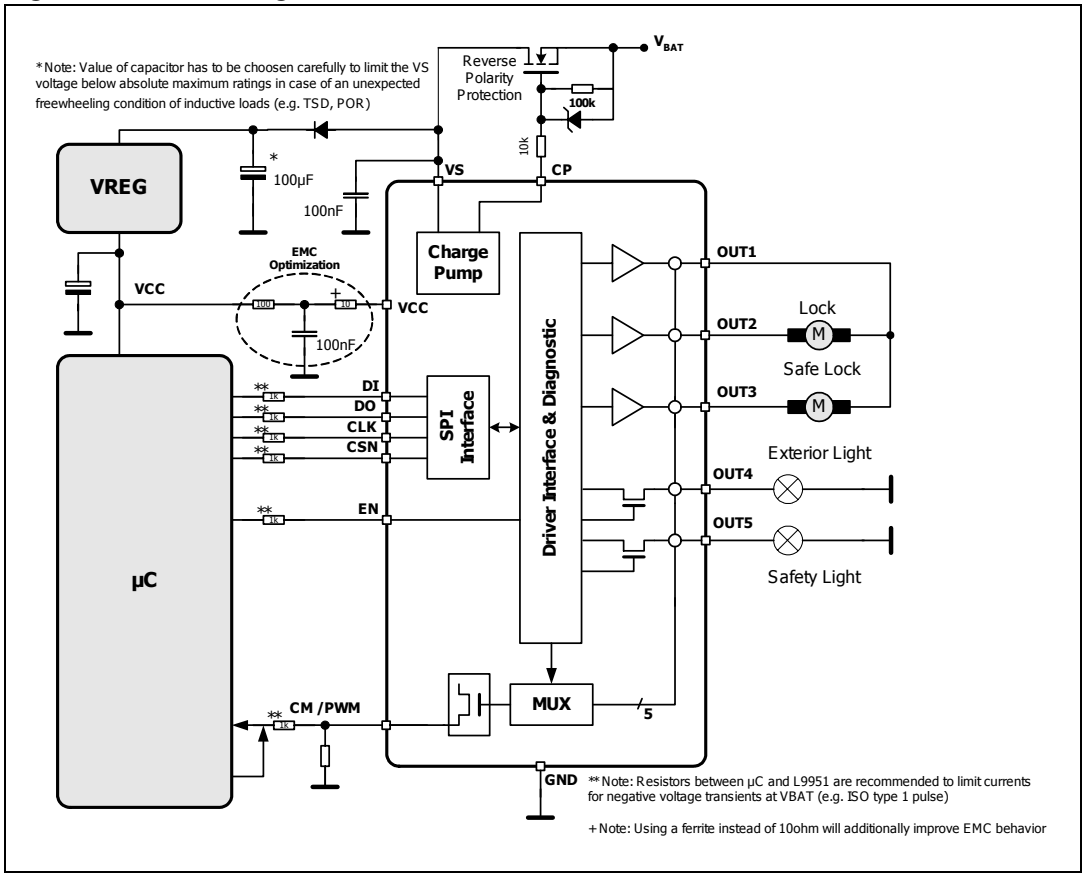


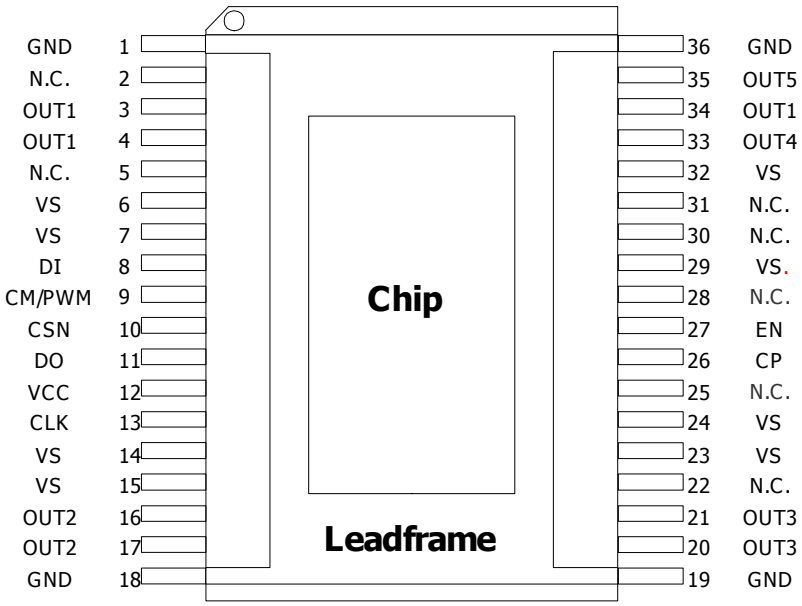
Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground . Reference potential. Note: For the capability of driving the full current at the outputs all pins of GND must be externally connected.
6, 7, 14, 15, 23, 24, 29, 32	VS	Power supply voltage (external reverse protection required). For EMI reason a ceramic capacitor as close as possible to GND is recommended. Note: for the capability of driving the full current at the outputs all pins of VS must be externally connected.
3, 4, 34	OUT1	Half-bridge output 1. The output is built by a high side and a low side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal reverse diode (bulk-drain-diode: high side driver from output to VS, low side driver from GND to output). This output is over-current and open load protected. Note: for the capability of driving the full current at the outputs all pins of OUT1 must be externally connected.
8	DI	Serial data input. The input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 16bit control word and the least significant bit (LSB, bit 0) is transferred first.
9	CM/PWM	Current monitor output/PWM input. Depending on the selected multiplexer bits (bit 9, 10, 11) of Input Data Register this output sources an image of the instant current through the corresponding high side driver with a ratio of 1/10.000. This pin is bidirectional. The microcontroller can overwrite the current monitor signal to provide a PWM input for all outputs. Testmode: If CSN is raised above 7.5V the device will enter the test mode. In test mode this output can be used to measure some internal signals (see *Table 18*).
10	CSN	Chip select not input / Testmode . This input is low active and requires CMOS logic levels. The serial data transfer between L9951 and micro controller is enabled by pulling the input CSN to low level. If an input voltage of more than 7.5V is applied to CSN pin the L9951 will be switched into a test mode.
11	DO	Serial data output . The diagnosis data is available via the SPI and this tristate-output. The output will remain in tristate, if the chip is not selected by the input CSN (CSN = high).
12	VCC	Logic supply voltage . For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input . This input controls the internal shift register of the SPI and requires CMOS logic levels.

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
16, 17	OUT2	Half-bridge output 2 (see OUT1 - pin 3, 4). Note**:** for the capability of driving the full current at the outputs all pins of OUT2 must be externally connected.
20, 21	OUT3	Half-bridge output 3 (see OUT1 - pin 3, 4). Note: for the capability of driving the full current at the outputs all pins of OUT3 must be externally connected.
26	CP	Charge Pump Output **.** This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection (see *Figure 1*).
27	EN	Enable input. If Enable input is forced to GND the device will enter Standby-Mode. The outputs will be switched off and all registers will be cleared
33, 35	OUT4, OUT5	High side driver output 4, 5 . The output is built by a high side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high side driver is a power DMOS transistor with an internal reverse diode from the output to VS (bulk-drain-diode). The output is over-current and open load protected.

Figure 2. Configuration diagram (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
	Single pulse t_{max} < 400ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI},V_{DO},V_{CLK},V_{CSN},V_{EN}	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{CM}	Current monitor output	-0.3 to V_{CC} + 0.3	V
V_{CP}	Charge pump output	-25 to V_S + 11	V
$I_{OUT1,2,3}$	Output current	±10	A
$I_{OUT4,5}$	Output current	±5	A

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	±4(1)	kV
Output pins: OUT1 - OUT5	±8(2)	kV

1. HBM according to CDF-AEC-Q100-002.
2. HBM with all unzapped pins grounded.

2.3 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

2.4 Temperature warning and thermal shutdown

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j increasing			150	°C
$T_{jTW\ OFF}$	Temperature warning threshold junction temperature	T_j decreasing	130			°C
$T_{jTW\ HYS}$	Temperature warning hysteresis			5		°K
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing			170	°C
$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	T_j decreasing	150			°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis			5		°K

2.5 Electrical characteristics

V_S = 8 to 16V, V_{CC} = 4.5 to 5.3V, T_j = - 40 to 150°C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage range		7		28	V
I_S	V_S DC supply current	V_S = 13V, V_{CC} = 5.0V active mode OUT1 - OUT5 floating		7	20	mA
	V_S quiescent supply current	V_S = 13V, V_{CC} = 0V standby mode OUT1 - OUT5 floating T_{test} =-40°C, 25°C		3	10	µA
		T_{test} = 130°C		6	20	µA
I_{CC}	V_{CC} DC supply current	V_S = 13V, V_{CC} = 5.0V CSN = V_{CC} active mode		1	3	mA
	V_{CC} quiescent supply current	V_S = 13V, V_{CC} = 5.0V CSN = V_{CC} standby mode OUT1 - OUT5 floating		1	3	µA
$I_S + I_{CC}$	Sum quiescent supply current	V_S = 13V, V_{CC} = 5.0V CSN = V_{CC} standby mode OUT1 - OUT5 floating		7	23	µA

Table 8. Overvoltage and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	VS UV-threshold voltage	V_S increasing	6.0		7.2	V
$V_{SUV\ OFF}$	VS UV-threshold voltage	V_S decreasing	5.4		6.5	V
$V_{SUV\ hyst}$	VS UV-hysteresis	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$		0.55		V
$V_{SOV\ OFF}$	VS OV-threshold voltage	V_S increasing	18		24.5	V
$V_{SOV\ ON}$	VS OV-threshold voltage	V_S decreasing	17.5			V
$V_{SOV\ hyst}$	VS OV-hysteresis	$V_{SOV\ OFF}$ - $V_{SOV\ ON}$		0.5		V
$V_{POR\ OFF}$	Power-on-reset threshold	V_{CC} increasing			4.4	V
$V_{POR\ ON}$	Power-on-reset threshold	V_{CC} decreasing	3.1			V
$V_{POR\ hyst}$	Power-on-reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.3		V

Table 9. Current monitor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range	V_{CC} = 5V	0		4	V
$I_{CM,r}$	Current monitor output ratio: I_{CM} / $I_{OUT1,2,3,4,5}$	0V ≤V_{CM} ≤4V, VCC=5V		1:10000		-
$I_{CM\ acc}$	Current monitor accuracy	0V ≤VCM≤4V, V_{CC}=5V, $I_{OUT1\text{-}5,low}$ =500mA $I_{OUT1,high}$ =6A $I_{OUT2,3,high}$ =4.9A $I_{OUT4,5,high}$ =1.2A (FS=full scale=600 µA)		4% + 1%FS	8% + 2%FS	-

Table 10. Charge pump output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S=8V, I_{CP} = -60µA	6		13	V
		V_S=10V, I_{CP} = -80µA	8		13	V
		V_S≥12V, I_{CP} = -100µA	10		13	V
I_{CP}	Charge pump output current	V_{CP} = V_S+10V V_S =13.5V	100	150	300	µA

Table 11. OUT 1 - OUT 5

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{ON\ OUT1}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, I_{OUT1} = ±3 A		150	200	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT1} = ±3 A		225	300	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT1} = ±3 A		150	200	mΩ
$R_{ON\ OUT2}$ $R_{ON\ OUT3}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT2,3}$ = ±3 A		200	270	mΩ
		V_S = 13.5 V, T_j = 125 °C, $I_{OUT2,3}$ = ±3 A		300	400	mΩ
		V_S = 8.0 V, T_j = 25 °C, $I_{OUT2,3}$ = ±3 A		200	270	mΩ
$r_{ON\ OUT4,}$ $r_{ON\ OUT5}$	On-resistance to supply or GND	VS = 13.5 V, T_j = 25 °C, $I_{OUT4,5}$ = ±0.8 A		800	1100	mΩ
		V_S = 13.5 V, T_j = 125 °C, $I_{OUT4,5}$ = ±0.8 A		1250	1700	mΩ
		V_S = 8.0 V, T_j = 25 °C, $I_{OUT4,5}$ = ±0.8 A		800	1100	mΩ
$\|I_{OUT1}\|$	Output current limitation to supply or GND	Sink and source	7.4		15.5	A
$\|I_{OUT2}\|$, $\|I_{OUT3}\|$	Output current limitation to supply or GND	Sink and source	5.0		10.5	A
$\|I_{OUT4}\|$, $\|I_{OUT5}\|$	Output current limitation to GND	Source	1.25		2.6	A
$t_{d\ ON\ H}$	Output delay time, highside driver on	V_S = 13.5 V, corresponding lowside driver is not active	20	40	90	µs
$t_{d\ OFF\ H}$	Output delay time, highside driver off	V_S = 13.5 V	80	200	300	µs
$t_{d\ ON\ L}$	Output delay time, lowside driver on	V_S = 13.5 V, corresponding highside driver is not active	20	60	80	µs
$t_{d\ OFF\ L}$	Output delay time, lowside driver off	V_S = 13.5 V	80	150	300	µs
$t_{D\ HL}$	Cross current protection time, source to sink	$t_{d\ ON\ L}$ - $t_{d\ OFF\ H}$,		200	400	µs
$t_{D\ LH}$	Cross current protection time, sink to source	$t_{d\ ON\ H}$ - $t_{d\ OFF\ L}$		200	400	µs
I_{QLH}	Switched-off output current highside drivers of OUT1-5	V_{OUT1-5} = 0V, standby mode	0	-2	-5	µA
		V_{OUT1-5} = 0V, active mode	-40	-15	0	µA

Table 11. OUT 1 - OUT 5 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{QLL}	Switched-off output current lowside drivers of OUT1-3	$V_{OUT1-3} = V_S$, standby mode	0	50	100	µA
		$V_{OUT1-3} = V_S$, active mode	-40	-15	0	µA
I_{OLD1}	Open load detection current of OUT1		70	160	240	mA
I_{OLD23}	Open load detection current of OUT2, OUT3		70	160	240	mA
I_{OLD45}	Open load detection current of OUT4 and OUT5		5	15	40	mA
t_{dOL}	Minimum duration of open load condition to set the status bit		500		3000	µs
t_{ISC}	Minimum duration of over-current condition to switch off the driver		10		100	µs
dV_{OUT1}/dt	Slew rate of OUT1	V_S =13.5 V I_{load} = ±1.5 A	0.1	0.2	0.4	V/µs
dV_{OUT23}/dt	Slew rate of OUT2, OUT3	V_S = 13.5 V I_{load} = ±1.5 A	0.1	0.2	0.4	V/µs
dV_{OUT45}/dt	Slew rate of OUT4, OUT5	V_S = 13.5 V I_{load} = - 0.8 A	0.1	0.2	0.4	V/µs

2.6 SPI - Electrical characteristics

(V_S = 8 to 16V, V_{CC} = 4.5 to 5.3V, T_j = - 40 to 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin).

Table 12. Delay time from standby to active mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Internal startup time	Switching from standby to active mode. Time until not Ready Bit goes low.		80	300	µs

Table 13. Inputs: CSN, CLK, PWM1/2 and DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{inL}	Input low level	V_{CC} = 5V	1.5	2.0		V
V_{inH}	Input high level	V_{CC} = 5V		3.0	3.5	V
V_{inHyst}	Input hysteresis	V_{CC} = 5V	0.5			V
$I_{CSN\ in}$	Pull up current at input CSN	V_{CSN} = 3.5V V_{CC} = 5V	-50	-25	-10	µA
$I_{CLK\ in}$	Pull down current at input CLK	V_{CLK} = 1.5V	10	25	50	µA
$I_{DI\ in}$	Pull down current at input DI	V_{DI} = 1.5V	10	25	50	µA
$I_{EN\ in}$	Pull down resistance at input EN		100	210	480	kΩ
C_{in}	Input capacitance at input CLK, DI and PWM	V_{CC} = 0 to 5.3V		10	15	pF

Note: Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 14. DI timing (see *Figure 3.* and *Figure 4.*)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	V_{CC} = 5V	1000			ns
t_{CLKH}	Clock high time	V_{CC} = 5V	400			ns
t_{CLKL}	Clock low time	V_{CC} = 5V	400			ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_{CC} = 5V	400			ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_{CC} = 5V	400			ns
$t_{set\ DI}$	DI setup time	V_{CC} = 5V	200			ns
$t_{hold\ time}$	DI hold time	V_{CC} = 5V	200			ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_{CC} = 5V			100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_{CC} = 5V			100	ns

Note: DI timing parameters tested in production by a passed/failed test:
Tj= -40°C/+25°C: SPI communication @2MHZ.
Tj= +125°C: SPI communication @1.25MHZ.

Table 15. DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	VCC = 5 V, I_D = -4mA		0.2	0.4	V
V_{DOH}	Output high level	VCC = 5 V, I_D = 4 mA	V_{CC} -0.4	V_{CC} -0.2		V
I_{DOLK}	Tristate leakage current	$V_{CSN} = V_{CC}$, 0V < V_{DO} < V_{CC}	-10		10	µA
C_{DO} (1)	Tristate input capacitance	$V_{CSN} = V_{CC}$, 0V < V_{CC} < 5.3V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 16. DO timing (see *Figure 5*, *Figure 6*)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{load} = -1mA		80	140	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{load} = 1mA		50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_L = 100 pF, I_{load} = 1mA pull-up load to V_{CC}		100	250	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_L = 100 pF, I_{load} = 4 mA pull-up load to V_{CC}		380	450	ns
$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_L =100 pF, I_{load} = -1mA pull-down load to GND		100	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_L = 100 pF, I_{load} = -4mA pull-down load to GND		380	450	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_{CC}, V_{DO} > 0.7V_{CC}, C_L = 100pF		50	250	ns

Table 17. EN, CSN timing (see *Figure 7*)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{EN\_CSN\_LO}$	Minimum EN high before sending first SPI frame, i.e. CSN going low	Transfer of SPI-command to input register		20	50	µs
$t_{CSN\_HI,min}$	Minimum CSN HI time between two SPI frames	Transfer of SPI-command to input register		2	4	µs

Figure 3. SPI - Transfer timing diagram

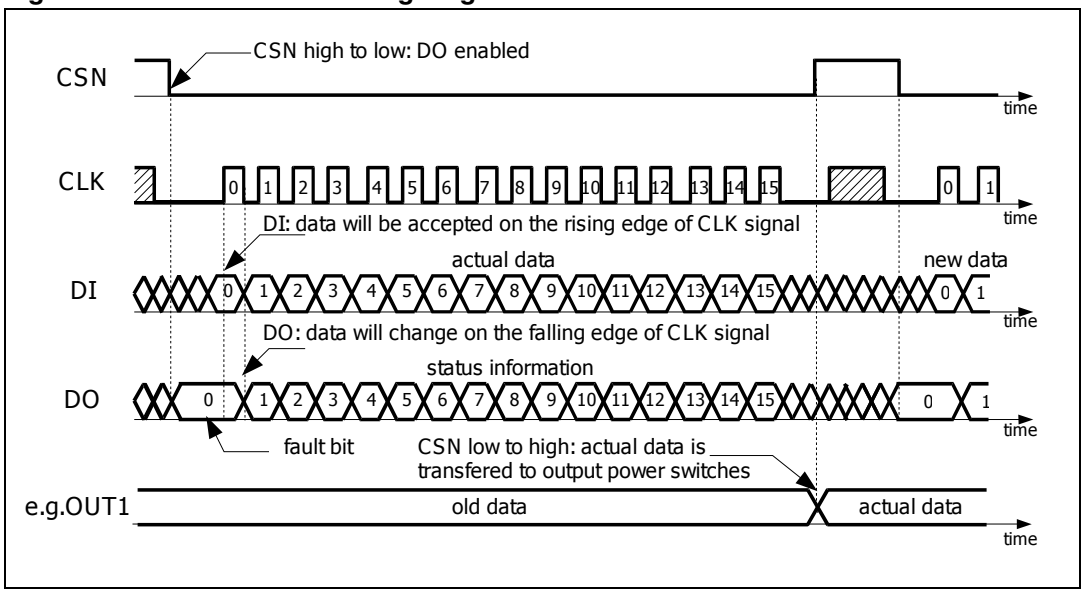


Figure 4. SPI - Input timing

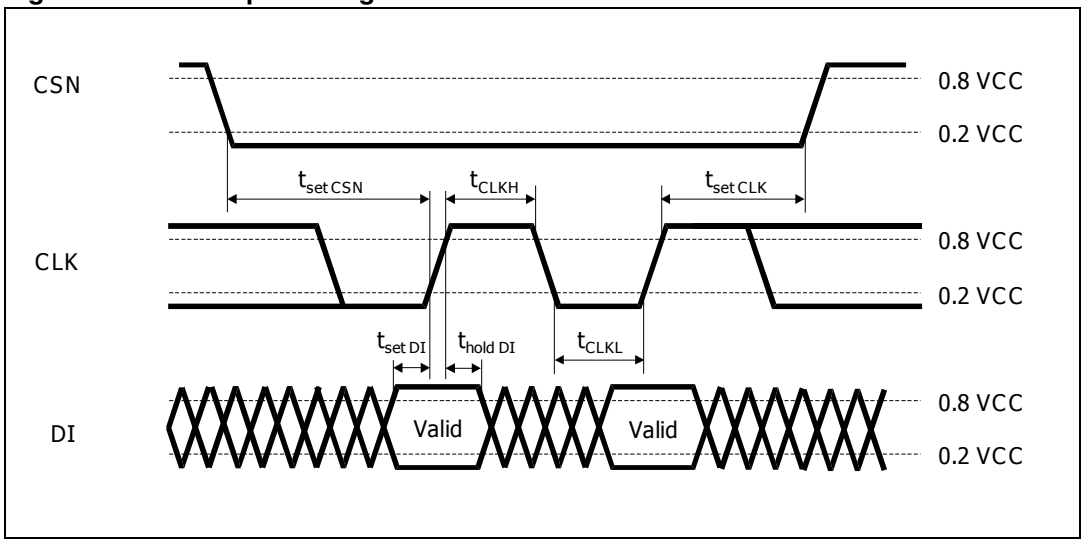


Figure 5. SPI - DO valid data delay time and valid time

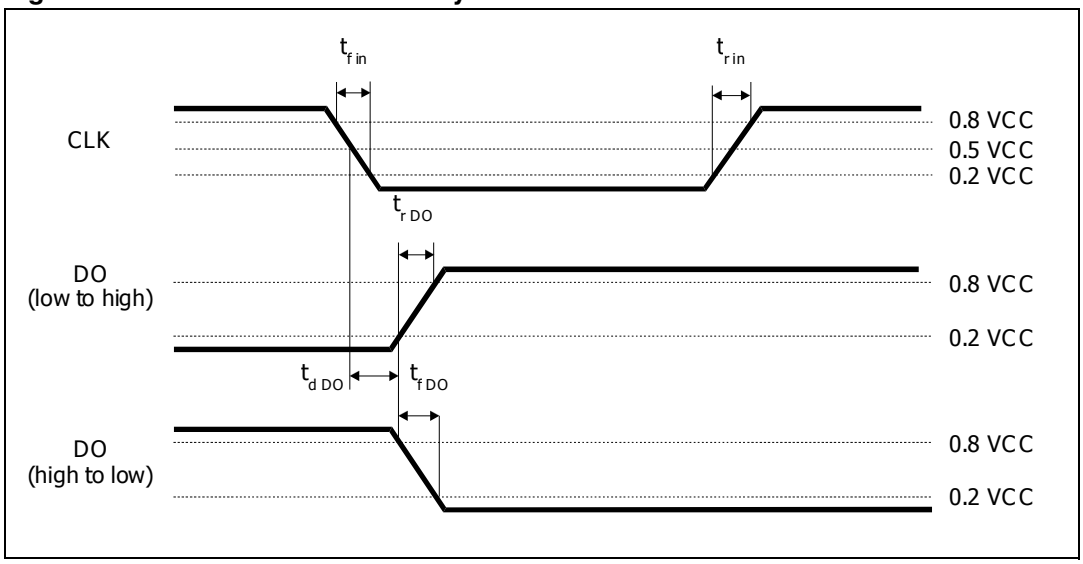


Figure 6. SPI - DO enable and disable time

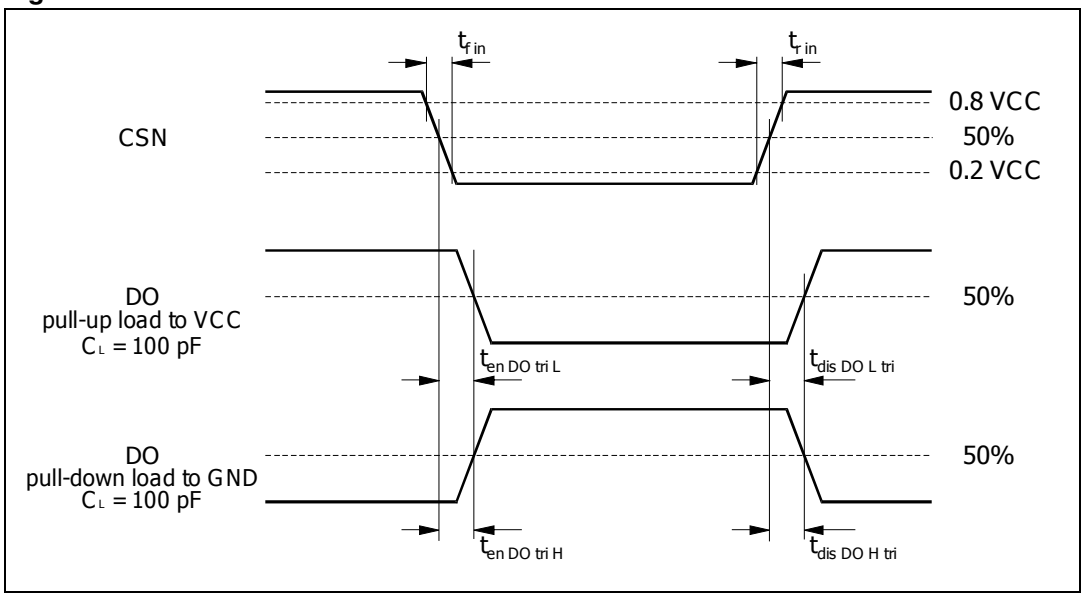


Figure 7. SPI - Driver turn on/off timing, minimum CSN HI time

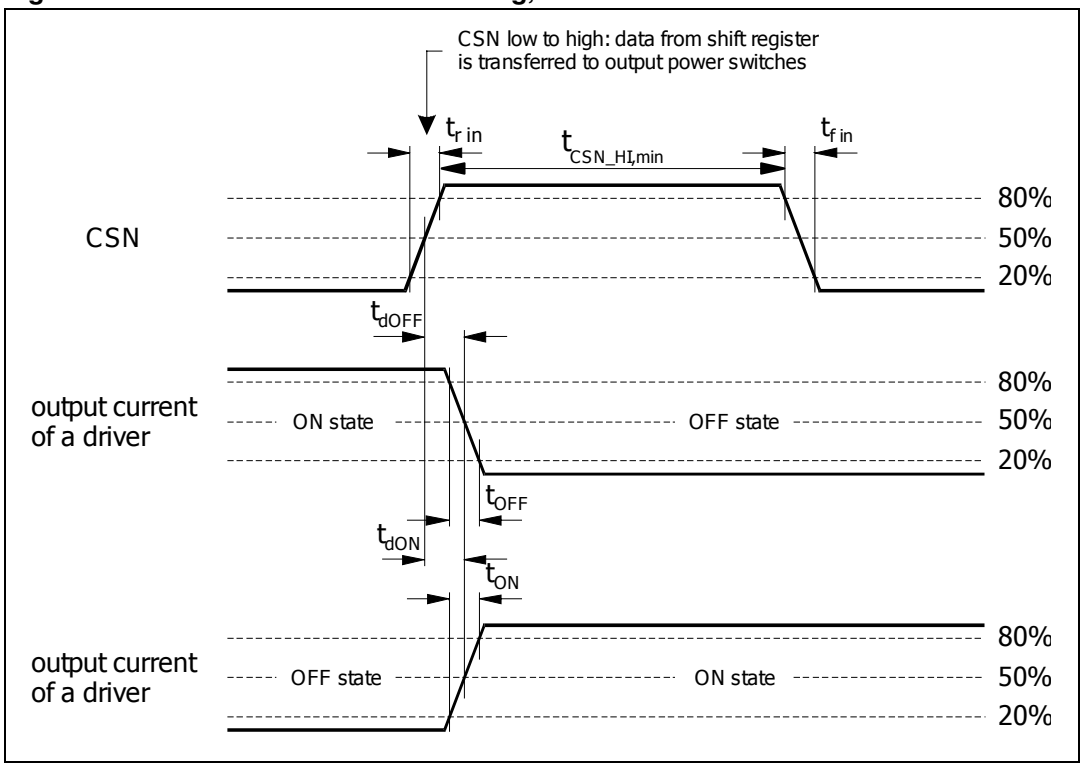
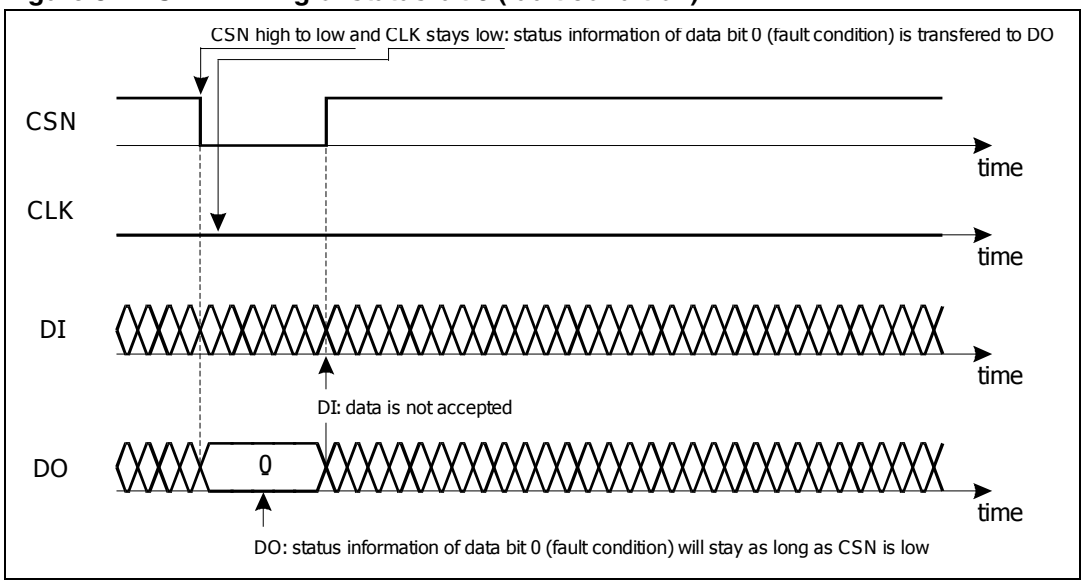


Figure 8. SPI - Timing of status bit 0 (fault condition)



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges and the high side drivers. An internal charge-pump is used to drive the high side switches. The logic supply voltage V_{CC} (stabilized 5V) is used for the logic part and the SPI of the device. Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (V_{CC} increases from under voltage to $V_{POR\ OFF}$ = 4.0V, typical) the circuit is initialized by an internally generated power-on-reset (POR).

If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ =3.6V, typical), the outputs are switched to tristate (high impedance) and the status registers are cleared.

3.2 Standby - mode

The standby mode of the L9951 is activated by switching the EN input do GND. All latched data will be cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at V_S (V_{CC}) is less than 3 µA (1µA) for CSN = high (DO in tristate). If EN is switched to 5V the device will enter the active mode. In the active mode the charge-pump and the supervisor functions are activated.

3.3 Inductive loads

Each half bridge is built by an internally connected high side and a low side power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT3 without external free-wheeling diodes. The high side drivers OUT4 to OUT5 are intended to drive resistive loads. Hence only a limited energy (E<0.5mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L > 50µH) an external free-wheeling diode connected to GND and the corresponding output is needed.

3.4 Diagnostic functions

All diagnostic functions (over/open load, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least 32µs (open load: 1ms, respectively) before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. Open load and temperature warning function are intended for information purpose and will not change the state of the output drivers. On contrary, the over load and thermal shutdown condition will disable the corresponding driver (over load) or all drivers (thermal shutdown), respectively. Without setting the over-current recovery bit in the Input Data Register to logic high, the microcontroller has to clear the over-current status bit to reactivate the corresponding driver. Each driver has a corresponding over-current recovery bit. If this bit is set, the device will automatically switch-on the outputs again after a short recovery time. The duty cycle in over-current condition can be programmed by the SPI interface (12% or 25%). With this feature the device can drive loads with start-up currents higher than the over-current limits (e.g. inrush current of lamps, cold resistance of motors and heaters).

3.5 Over-voltage and under-voltage detection

If the power supply voltage V_S rises above the over-voltage threshold $V_{SOV\ OFF}$ (typical 21V), the outputs OUT1 to OUT5 are switched to high impedance state to protect the load and the internal charge-pump is turned-off. When the voltage V_S drops below the undervoltage threshold $V_{SUV\ OFF}$ (UV-switch-OFF voltage), the output stages are switched to the high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S recovers to normal operating voltage the output stages return to the programmed state (input register 0: bit 12=0). If the undervoltage / overvoltage recovery disable bit is set, the automatic turn-on of the drivers is deactivated. The microcontroller needs to clear the status bits to reactivate the drivers.

3.6 Temperature warning and thermal shutdown

If junction temperature rises above $T_{j\ TW}$ a temperature warning flag is set and is detectable via the SPI. If junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit will be set and power DMOS transistors of all output stages are switched off to protect the device. In order to reactivate the output stages the junction temperature must decrease below T_{jSD} - $T_{jSD\ HYS}$ and the thermal shutdown bit has to be cleared by the microcontroller.

3.7 Open load detection

The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.

3.8 Over load detection

In case of an over-current condition a flag is set in the status register in the same way as open load detection. If the over-current signal is valid for at least t_{ISC}=32µs, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.9 Current monitor

The current monitor output sources a current image at the current monitor output which has a fixed ratio (1/10000) of the instantaneous current of the selected high side driver. The bits 9, 10 and 11 of the input data register 0 control which of the outputs OUT1 to OUT5 will be multiplexed to the current monitor output. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example this can be used to detect the motor state (starting, free-running, stalled). Moreover, it is possible to regulate the power of the defroster more precise by measuring the monitor current.

3.10 PWM input

Each driver has a corresponding PWM enable bit which can be programmed by the SPI interface. If the PWM enable bit is set, the outputs OUT1 to OUT5 are controlled by the logically AND-combination of the signal applied to the PWM input and the output control bit in input data register1.

3.11 Cross-current protection

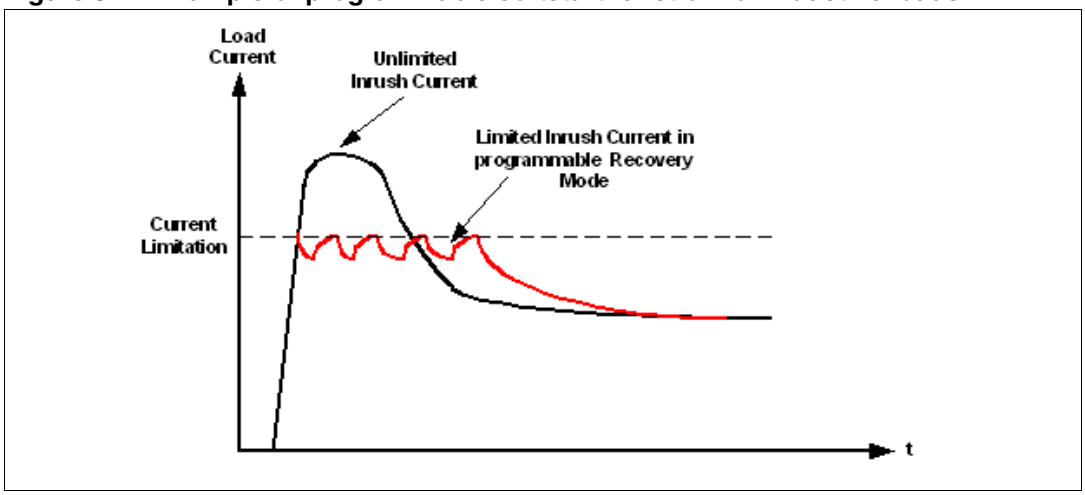
The three half-brides of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge will be automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver will be changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver will start to conduct.

3.12 Programmable softstart function to drive loads with higher inrush current

Loads with start-up currents higher than the over-current limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable softstart function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device will automatically switch-on the outputs again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to be about 12% or 25%. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition.

The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example the microcontroller can switch on light bulbs by setting the over-current Recovery bit for the first 50ms. After clearing the recovery bit the output will be automatically disabled if the overload condition still exits.

Figure 9. Example of programmable softstart function for inductive loads



4 Functional description of the SPI

4.1 Serial Peripheral Interface (SPI)

This device uses a standard SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect the status bit 0 (fault condition) of the device which is a logical-or of all bits in the status registers 0 and 1. The microcontroller can poll the status of the device without the need of a full SPI-communication cycle.

Note: In contrast to the SPI-standard the least significant bit (LSB) will be transferred first (see Figure 3).

4.2 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal will activate the output driver and a serial communication can be started.

The state when CSN is going low until the rising edge of CSN will be called a communication frame. If the CSN-input pin is driven above 7.5V, the L9951 will go into a test mode. In the test mode the DO will go from tristate to active mode.

4.3 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 16 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transferred to Data Input Register.

The writing to the selected Data Input Register is only enabled if exactly 16 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.4 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

4.5 Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal.

4.6 Input data register

The device has two input registers. The first bit (bit 0) at the DI-input is used to select one of the two input registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected input data register only if a frame of exact 16 data bits are detected. Depending on bit 0 the contents of the selected status register will be transferred to DO during the current communication frame. Bit 1-8 control the behavior of the corresponding driver. The bits 9,10 and 11 are used to control the current monitor multiplexer. Bit 15 is used to reset all status bits in both status registers. The bits in the status registers will be cleared after the current communication frame (rising edge of CSN).

4.7 Status register

This devices uses two status registers to store and to monitor the state of the device. Bit 0 is used as a fault bit and is a logical-NOR combination of bits 1-14 in both status registers. The state of this bit can be polled by the microcontroller without the need of a full SPI-communication cycle (see *Figure 8.*). If one of the over-current bits is set, the corresponding driver will be disabled. If the over-current recovery bit of the output is not set the microcontroller has to clear the over-current bit to enable the driver. If the thermal shutdown bit is set, all drivers will go into a high impedance state. Again the microcontroller has to clear the bit to enable the drivers.

4.8 Test mode

The test mode can be entered by rising the CSN input to a voltage higher than 7.5V. In the test mode the inputs CLK, DI, PWM and the internal 2MHz CLK can be multiplexed to data output DO for testing purpose. Furthermore the over-current thresholds are reduced by a factor of 4 to allow EWS testing at lower current. The internal logic prevents that the Hi-Side and Low-Side driver of the same half-bridge can be switched-on at the same time. In the test mode this combination is used to multiplex the desired signals to the CM output according to table 18 and 19.

Table 18. Test mode

LS1 HS1	LS2 HS2	LS3 HS3	DO	LS1 HS1	LS2 HS2	LS3 HS3	CM
! (both HI)	! (both HI)	! (both HI)	NoError	! (both HI)	! (both HI)	! (both HI)	N.C
both HI	! (both HI)	! (both HI)	DI	both HI	! (both HI)	! (both HI)	Tsense1
! (both HI)	both HI	! (both HI)	CLK	! (both HI)	both HI	! (both HI)	Tsense2
both HI	both HI	! (both HI)	INT_CLK	both HI	both HI	! (both HI)	Tsense3
! (both HI)	! (both HI)	both HI	PWM	! (both HI)	! (both HI)	both HI	Tsense4
				both HI	! (both HI)	both HI	N.C
				! (both HI)	both HI	both HI	5µA Iref
				both HI	both HI	both HI	Vbandgap

Table 19. SPI - Input data and status register 0

Input register 0 (write)			Status register 0 (read)	
Bit	**Name**	**Comment**	**Name**	**Comment**
15	Reset bit	If reset bit is set both status registers will be cleared after rising edge of CSN input.	Always 1	A broken VCC-or SPI-connection of the L9951 can be detected by the microcontroller, because all 16 bits low or high is not a valid frame.
14	Disable open load	If the disable open load bit is set, the open load status bits will be ignored for the NonErrorBit calculation.	V_S over-voltage	In case of an over-voltage or undervoltage event the corresponding bit is set and the outputs are deactivated.
13	OC recovery duty cycle 0: 12% 1: 25%	This bit defines in combination with the over-current recovery bit (input register 1) the duty cycle in over-current condition of an activated driver. If temperature warning bit is set, L9951 will always use the lower duty cycle	V_S undervoltage	If VS voltage recovers to normal operating conditions outputs are reactivated automatically.
12	Overvoltage/ under-voltage recovery disable	If this bit is set the microcontroller has to clear the status register after undervoltage/overvoltage event to enable the outputs.	Thermal shutdown	In case of an thermal shutdown all outputs are switched off. The microcontroller has to clear the TSD bit by setting the reset bit to reactivate the outputs.

Table 19. SPI - Input data and status register 0 (continued)

<table>
<tr><th rowspan="2">Bit</th><th colspan="2">Input register 0 (write)</th><th colspan="2">Status register 0 (read)</th></tr>
<tr><th>Name</th><th>Comment</th><th>Name</th><th>Comment</th></tr>
<tr><td>11</td><td rowspan="2">Current monitor select bits</td><td rowspan="2">Following current image (1/10.000) of the HS driver will be multiplexed to CM output:
<table><tr><th>Bit 11</th><th>Bit 10</th><th>Bit 9</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>0</td><td>OUT1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>OUT2</td></tr><tr><td>0</td><td>1</td><td>0</td><td>OUT3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>OUT4</td></tr><tr><td>1</td><td>0</td><td>0</td><td>OUT5</td></tr></table></td><td>Temperature warning</td><td>This bit is for information purpose only. It can be used for a thermal management by the microcontroller to avoid a thermal shutdown.</td></tr>
<tr><td>10</td><td>Not ready bit</td><td>After switching the device from standby mode to active mode an internal timer is started to allow charge pump to settle before the outputs can be activated. This bit is cleared automatically after start up time has finished. Since this bit is controlled by internal clock it can be used for synchronizing testing events (e.g. measuring filter times).</td></tr>
<tr><td>9</td><td></td><td></td><td>0</td><td>Not used</td></tr>
<tr><td>8</td><td>OUT5 - HS on/off</td><td rowspan="8">If a bit is set the selected output driver is switched on. If the corresponding PWM enable bit is set (Input Register 1) the driver is only activated if PWM input signal is high. The outputs of OUT1-OUT3 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from VS to GND.</td><td>OUT5-HS over - current</td><td rowspan="8">In case of an over-current event the corresponding status bit is set and the output driver is disabled. If the over-current recovery enable bit is set (Input Register 1) the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (Bit 13).
If the over-current recovery bit is not set the microcontroller has to clear the over-current bit (reset bit) to reactivate the output driver.</td></tr>
<tr><td>7</td><td>OUT4 - HS on/off</td><td>OUT4-HS over - current</td></tr>
<tr><td>6</td><td>OUT3 - HS on/off</td><td>OUT3-HS over - current</td></tr>
<tr><td>5</td><td>OUT3 - LS on/off</td><td>OUT3-LS over - current</td></tr>
<tr><td>4</td><td>OUT2 - HS on/off</td><td>OUT2-HS over - current</td></tr>
<tr><td>3</td><td>OUT2 - LS on/off</td><td>OUT2-LS over - current</td></tr>
<tr><td>2</td><td>OUT1 - HS on/off</td><td>OUT1-HS over - current</td></tr>
<tr><td>1</td><td>OUT1 - LS on/off</td><td>OUT1-LS over - current</td></tr>
<tr><td>0</td><td colspan="2">0</td><td>No error bit</td><td>A logical NOR-combination of all bits 1 to 14 in both status registers. If bit 14 (disable open-load) is set, the open-load status will be ignored.</td></tr>
</table>

Table 20. SPI - Input data and status register 1

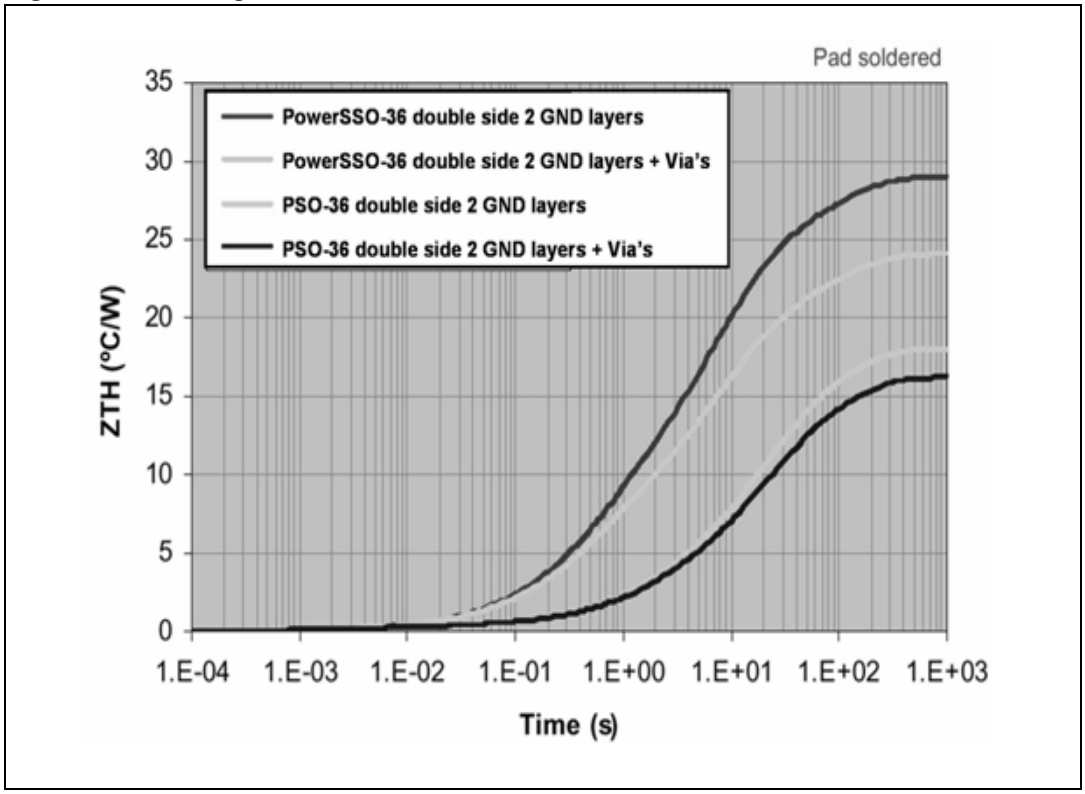
Input register 1 (write)			Status register 1 (read)	
Bit	**Name**	**Comment**	**Name**	**Comment**
15	Not used		Always 1	A broken VCC-or SPI-connection of the L9951 can be detected by the microcontroller, because all 16 bits low or high is not a valid frame.
14	Not used		V_S over-voltage	In case of an over-voltage or undervoltage event the corresponding bit is set and the outputs are deactivated.
13	Not used		V_S undervoltage	In case of an over-voltage or undervoltage event the corresponding bit is set and the outputs are deactivated.
12	Not used		Thermal shutdown	In case of an thermal shutdown all outputs are switched off. The microcontroller has to clear the TSD bit by setting the reset bit to reactivate the outputs.
11	Not used		Temperature warning	This bit is for information purpose only. It can be used for a thermal management by the microcontroller to avoid a thermal shutdown.

Table 20. SPI - Input data and status register 1 (continued)

Input register 1 (write)			Status register 1 (read)	
Bit	**Name**	**Comment**	**Name**	**Comment**
10	OUT5 OC recovery enable	In case of an over-current event the over-current status bit (status register 0) is set and the output is switched off. If the over-current recovery enable bit is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (Bit 13 of Input data register 1). Depending on occurrence of overcurrent event and internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero.	Not ready bit	After switching the device from standby mode to active mode an internal timer is started to allow charge pump to settle before the outputs can be activated. This bit is cleared automatically after start up time has finished. Since this bit is controlled by internal clock it can be used for synchronizing testing events(e.g. measuring filter times).
9	OUT4 OC recovery enable		0	Not used.
8	OUT3 OC recovery enable		OUT5-HS open load	The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set. Due to mechanical /electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.
7	OUT2 OC recovery enable		OUT4-HS open load	
6	OUT1 OC recovery enable		OUT3-HS open load	
5	OUT5 PWM enable	If the PWM enable bit is set and the output is enabled (input register 0) the output is switched on if PWM input is high and switched off if PWM input is low.	OUT3-LS open load	
4	OUT4 PWM enable		OUT2-HS open load	
3	OUT3 PWM enable		OUT2-LS open load	
2	OUT2 PWM enable		OUT1-HS open load	
1	OUT1 PWM enable		OUT1-LS open load	
0	1		No error bit	A logical NOR-combination of all bits 1 to 14 in both status registers. If bit 14 (Disable Open-Load) is set, the open-load status will be ignored

5 Packages thermal data

Figure 10. Packages thermal data



6 Package and packing information

6.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

6.2 PowerSO-36™ package information

Figure 11. PowerSO-36™ package dimensions

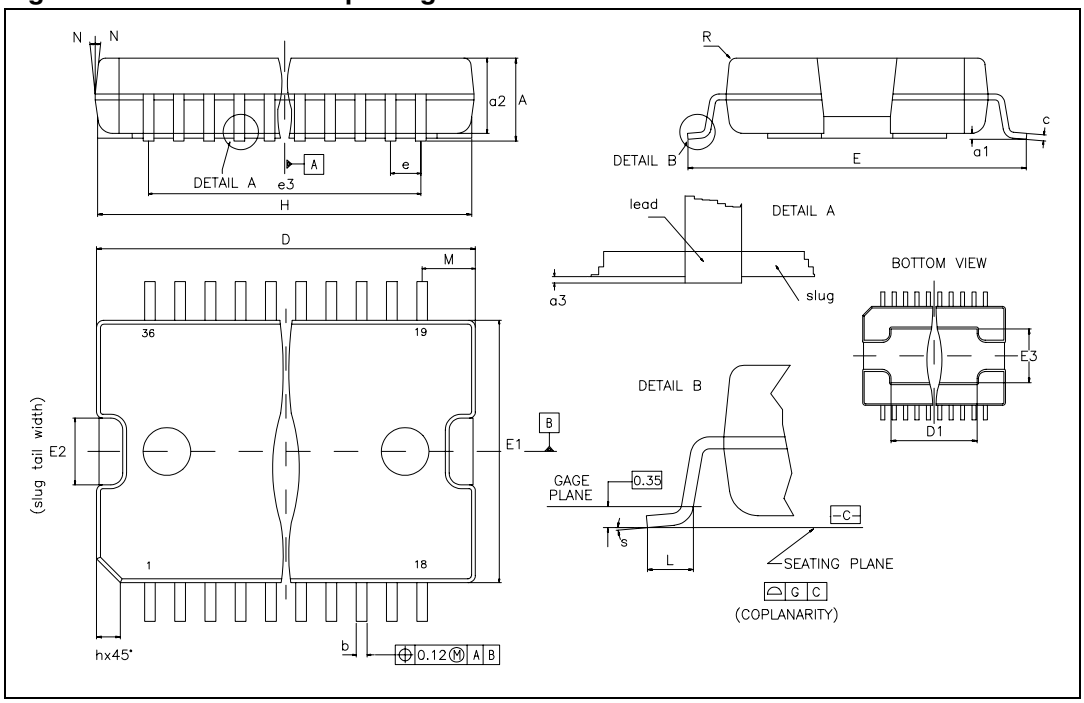


Table 21. PowerSO-36™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			3.60
a1	0.10		0.30
a2			3.30
a3	0		0.10
b	0.22		0.38
c	0.23		0.32
D *	15.80		16.00
D1	9.40		9.80
E	13.90		14.5
E1 *	10.90		11.10
E2			2.90
E3	5.80		6.20
e		0.65	
e3		11.05	
G	0		0.10
H	15.50		15.90
h			1.10
L	0.8		1.10
M			
N			10 deg
R			
s			8 deg

6.3 PowerSSO-36™ package information

Figure 12. PowerSSO-36™ package dimensions

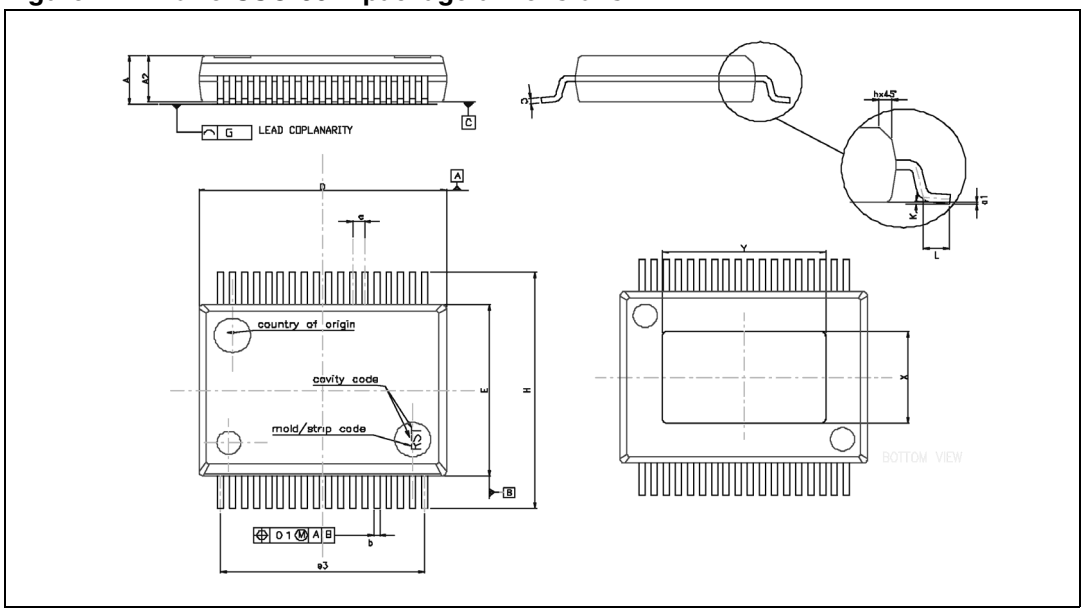


Table 22. PowerSSO-36™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.47
A2	2.15	-	2.40
a1	0	-	0.075
b	0.18	-	0.36
c	0.23	-	0.32
D *	10.10	-	10.50
E *	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
L	0.55	-	0.85
N	-	-	10 deg
X	4.1	-	4.7
Y	6.5	-	7.1

6.4 PowerSO-36™ packing information

Figure 13. PowerSO-36™ tube shipment (no suffix)

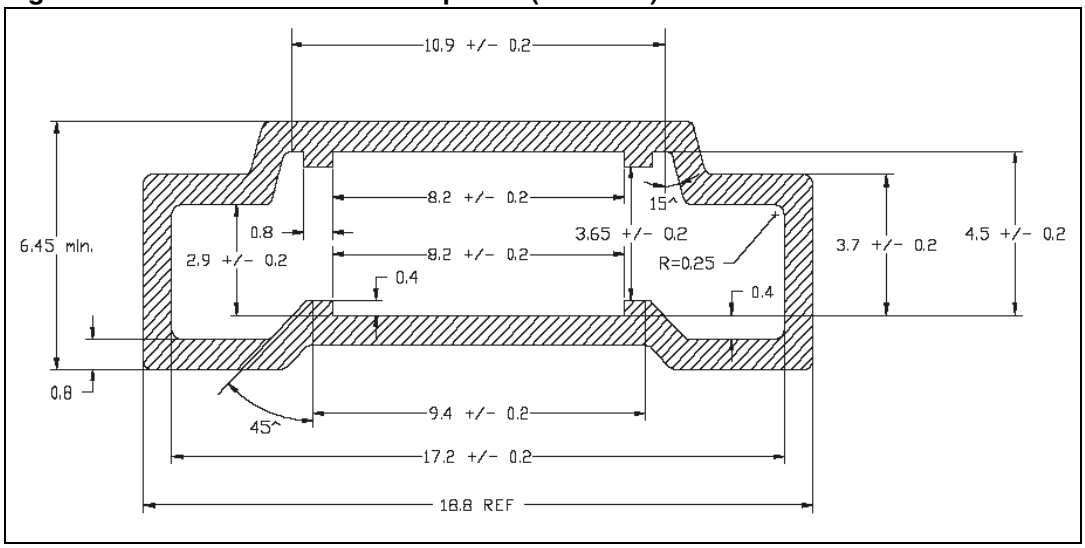
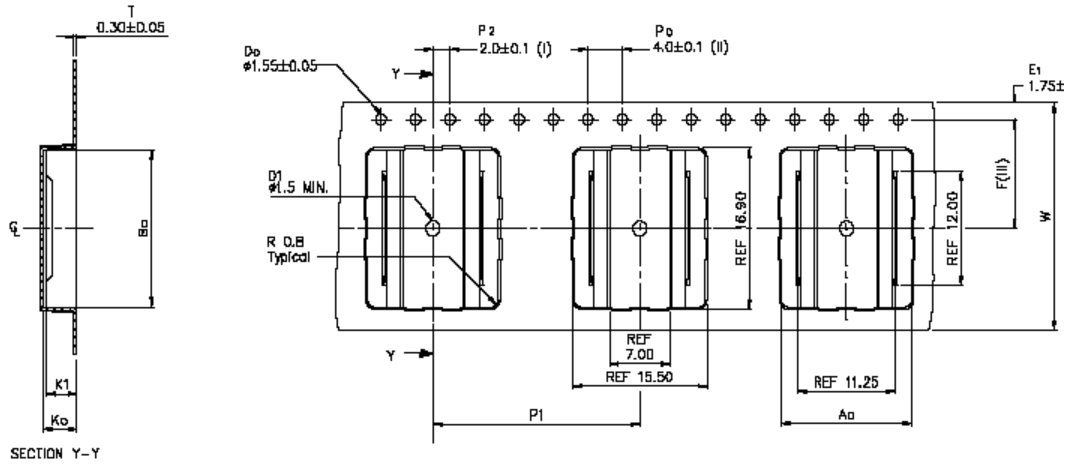
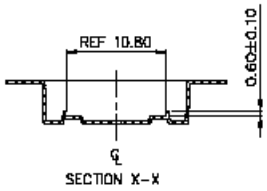


Figure 14. PowerSO-36™ tape and reel shipment (suffix "TR")





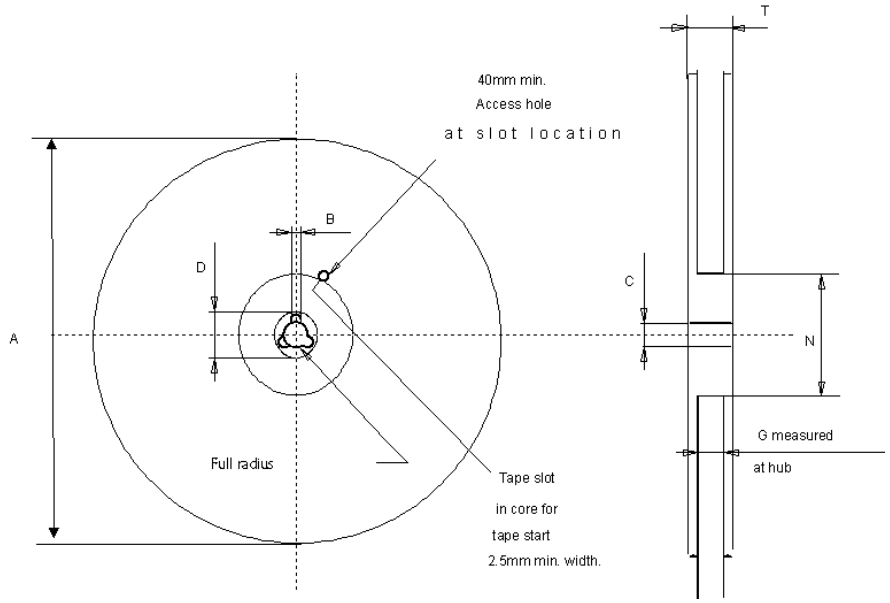
TAPE DIMENSIONS

A0	15.20 ± 0.1
B0	16.60 ± 0.1
K0	3.90 ± 0.1
K1	3.50 ± 0.1
F	11.50 ± 0.1
P1	24.00 ± 0.1
W	24.00 ± 0.3

All dimensions are in mm.

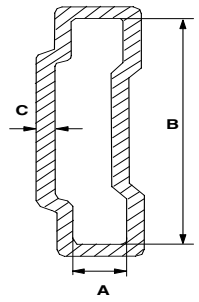
REEL DIMENSIONS

Base Qty	600
Bulk Qty	600
A (max)	330
B (min)	1.5
C (±0.2)	13
D (min)	20.2
G (+2 / -0)	24.4
N (min)	60
T (max)	30.4



6.5 PowerSSO-36™ packing information

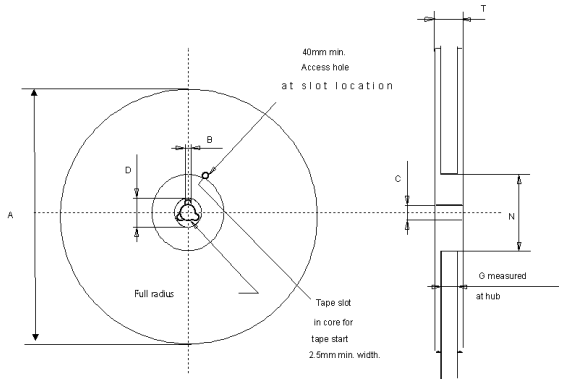
Figure 15. PowerSSO-36™ tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 16. PowerSSO-36™ tape and reel shipment (suffix "TR")



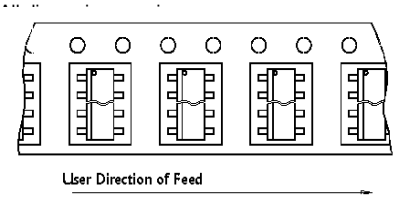
REEL DIMENSIONS

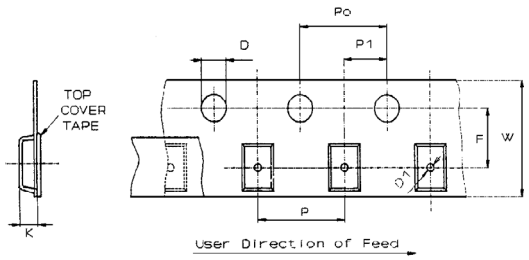
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

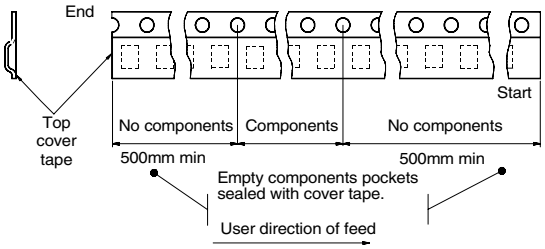
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2







7 Revision history

Table 23. Document revision history

Date	Revision	Description of changes
Mar-2004	1	First issue
Jun-2005	2	Added *PowerSO-36™ package information*, *PowerSO-36™ package information*.
Jul-2005	3	Updated *Figure 1.: Block diagram* .
Sep-2005	4	Note 1 removal; Updated *Figure 10.: Packages thermal data*.
Feb-2006	5	Updated *Table 4.: ESD protection*.
15-Nov-2007	6	Document restructured and reformatted. Added *PowerSO-36™ packing information* and *PowerSSO-36™ packing information*.

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